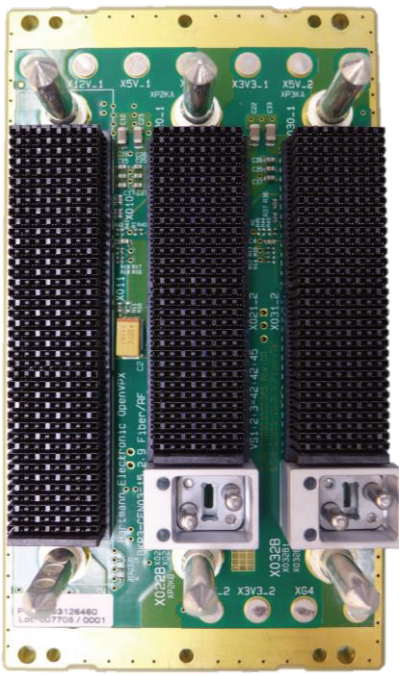
3U OpenVPX BACKPLANE with Fibre Optic Extension **BKP3-CEN03-15.3.5-3**	**VITA 46** **VITA 65** **VITA 66.4**	

Key Features:

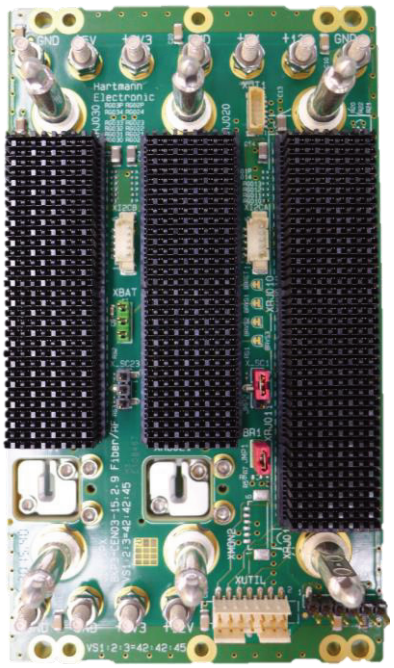
- Compliant to VITA 46.0 baseline specification
- Compliant to VITA 65 OpenVPX, BKP3-CEN03-15.3.5-3
- Compliant to VITA 66.4 Optical Interconnect On VPX
- 1+2 Slots VPX, 1 Payload Slot, 2 Payload Slots with optical
- Single Star X4 (2 FPs) configuration for Data Plane
- M3 studs for power entry
- PCB size 128.50 mm x 73.05 mm x 5.4 mm
- 5 HP from slot to slot (25.40 mm)
- Flexible keying and alignment mechanism
- with geographical address pins
- Reference clock
- Auxilary clock
- System Reset
- With JTAG connector on first slot (JT1)
- System Management Interface on the backplane (I2CA, I2CB)
- Non-Volatile Memory Read Only signal set by Jumper BR1
- Battery backup option setting by Jumper XBAT. Vbat external or connected to 3.3 VAUX.
- Max. Input current per backplane VS1:VS2:VS3 = 42A : 42A : 45A
- Operating temperature: -40°C - +85°C
- Storage temperature: -55°C - +85°C
- Flammability rating: UL94-V0
- Custom assembly or modification on request

- **Order number: B193126460**

Front side



Back side

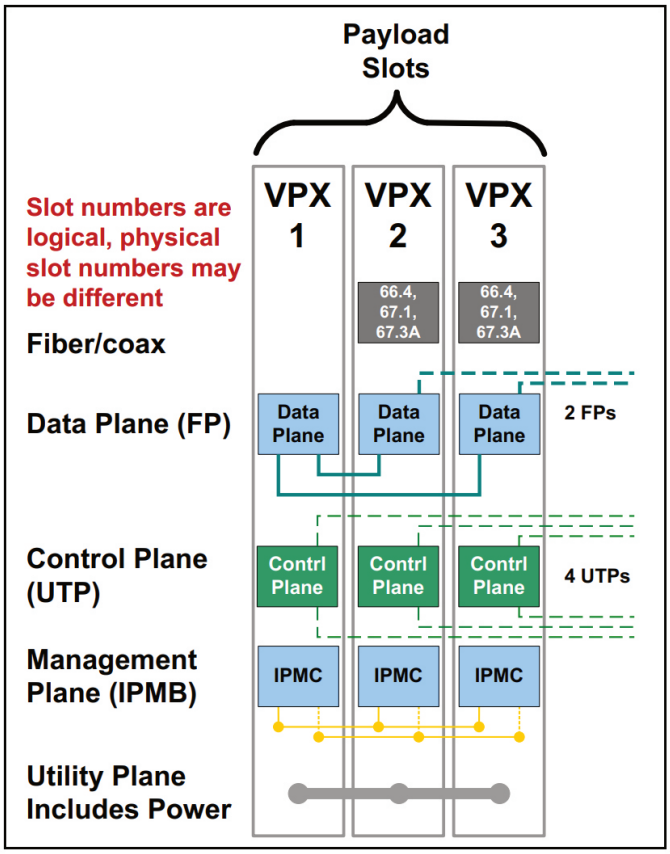


3U OpenVPX BACKPLANE with Fibre Optic Extension **BKP3-CEN03-15.3.5-3**	**VITA 46** **VITA 65** **VITA 66.4**	

1) Topology: 3-Slot — BKP3-CEN03-15.3.5-3 (1 Payload + 2 Payload with optical)

Profile Payload slot without optical: SLT3-PAY-2F2U-14.2.3 / MOD3-PAY-2F2U-16.2.3

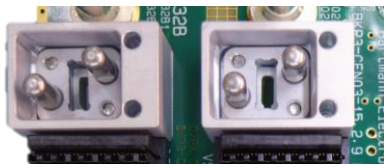
Profile Payload slot with optical : SLT3-PAY-2F2U1E-14.6.10 / MOD3-PAY-2F2U1E-16.6.10

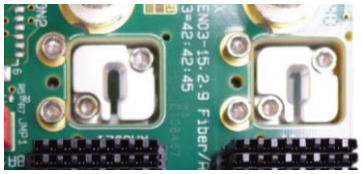


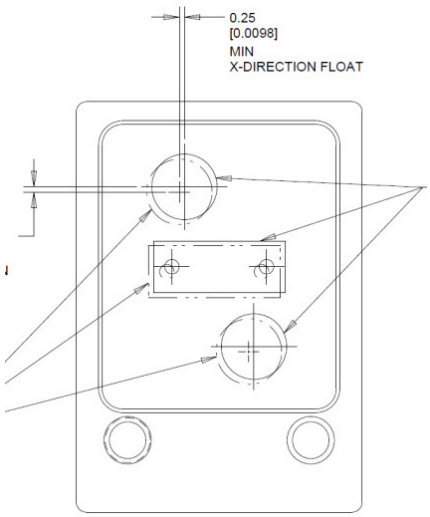
2) Fibre Optic Extension

This Backplance features VITA 66.4 fibre Connector Modules in two of the slots.

Optical Backplane Module by Tyco (item number 2226880-1)



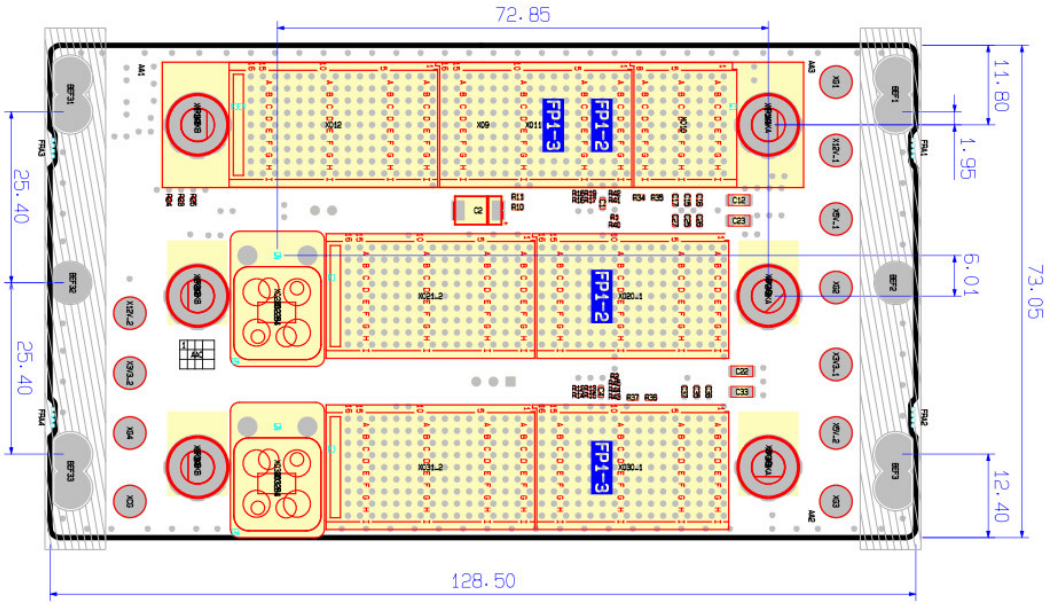




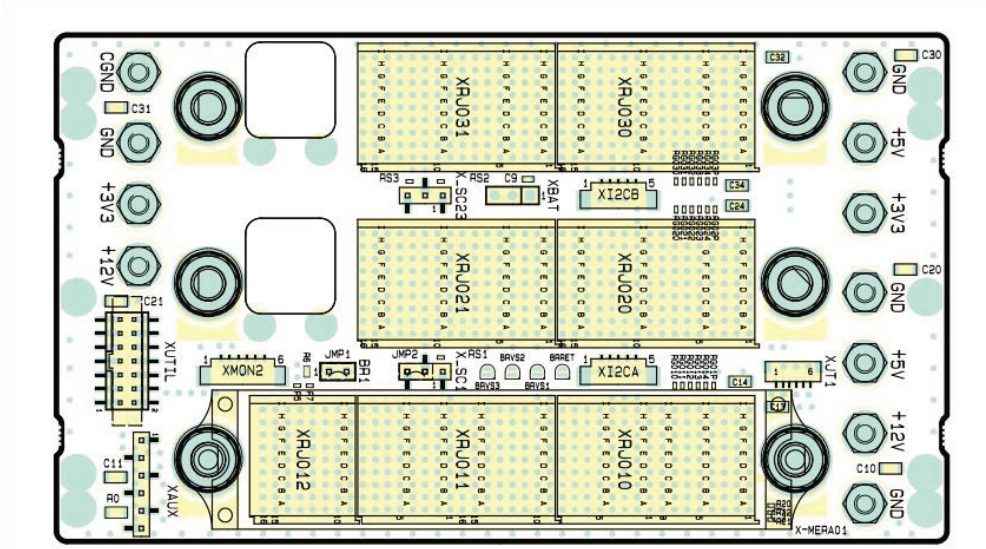
3U OpenVPX BACKPLANE with Fibre Optic Extension **BKP3-CEN03-15.3.5-3**	**VITA 46** **VITA 65** **VITA 66.4**	

3) Drawings

Front side



Back side





4) Pin Assignment

Pin Assignment VPX J0 (Utility Connector)

	Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Vs1	Vs1	Vs1	Vs1	No Pad*	Vs2	Vs2	Vs2	Vs2
2	Vs1	Vs1	Vs1	Vs1	No Pad*	Vs2	Vs2	Vs2	Vs2
3	Vs3	Vs3	Vs3	Vs3	No Pad*	Vs3	Vs3	Vs3	Vs3
4	GND	SM2	SM3	GND	-12V_Aux	GND	SYSRESET*	NVMRO	GND
5	GND	GAP*	GA4*	GND	3.3V_Aux	GND	SM0	SM1	GND
6	GND	GA3*	GA2*	GND	+12V_Aux	GND	GA1*	GA0*	GND
7	TCK	GND	GND	TDO	TDI	GND	GND	TMS	TRST*
8	GND	REF_CLK-	REF_CLK+	GND	GND	AUX_CLK-	AUX_CLK+	GND	GND

VS1=12V , VS2=3.3V , VS3=5V

Payload Slot Profile without optical SLT3-PAY-2F2U-14.2.3— P1 & J1

Plug-in module P1			Row G	Row F	Row E Even	Row E Odd	Row D	Row C	Row B Even	Row B Odd	Row A
Bplane J1			Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Data Plane Port 1	X8 x4 / 2x2 / 4x1	GDiscrete1	GND	GND-J1	DP01-TD0-	DP01-TD0+	GND	GND-J1	DP01-RD0-	DP01-RD0+
2			GND	DP01-TD1-	DP01-TD1+	GND-J1	GND	DP01-RD1-	DP01-RD1+	GND-J1	GND
3			P1-VBAT	GND	GND-J1	DP01-TD2-	DP01-TD2+	GND	GND-J1	DP01-RD2-	DP01-RD2+
4			GND	DP01-TD3-	DP01-TD3+	GND-J1	GND	DP01-RD3-	DP01-RD3+	GND-J1	GND
5	Data Plane Port 2	X8 x4 / 2x2 / 4x1	SYS_CON*	GND	GND-J1	DP02-TD0-	DP02-TD0+	GND	GND-J1	DP02-RD0-	DP02-RD0+
6			GND	DP02-TD1-	DP02-TD1+	GND-J1	GND	DP02-RD1-	DP02-RD1+	GND-J1	GND
7			Reserved	GND	GND-J1	DP02-TD2-	DP02-TD2+	GND	GND-J1	DP02-RD2-	DP02-RD2+
8			GND	DP02-TD3-	DP02-TD3+	GND-J1	GND	DP02-RD3-	DP02-RD3+	GND-J1	GND
9	User Defined		UD	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
10			GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
11			UD	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
12			GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
13			UD	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
14			GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
15	Control Plane		Maskable Reset*	GND	GND-J1	CPutp02-TD-	CPutp02-TD+	GND	GND-J1	CPutp02-RD-	CPutp02-RD+
16			GND	CPutp01-TD-	CPutp01-TD+	GND-J1	GND	CPutp01-RD-	CPutp01-RD+	GND-J1	GND



Payload Slot Profile without optical SLT3-PAY-2F2U-14.2.3— P2 & J2

This connector is all User Defined pins. See Section VITA 65 6.3.3 for requirements and pin assignments Concerning connectors that are all User Defined.
Connector Example Combined Plug-In Module & Backplane - Differential

Backplane Jn	Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	UD	UD	UD	UD	UD	GND	UD	UD	UD
2	GND	UD	UD	GND	UD	UD	UD	UD	GND
3	UD	UD	UD	UD	UD	GND	UD	UD	UD
4	GND	UD	UD	GND	UD	UD	UD	UD	GND
5	UD	UD	UD	UD	UD	GND	UD	UD	UD
6	GND	UD	UD	GND	UD	UD	UD	UD	GND
7	UD	UD	UD	UD	UD	GND	UD	UD	UD
8	GND	UD	UD	GND	UD	UD	UD	UD	GND
9	UD	UD	UD	UD	UD	GND	UD	UD	UD
10	GND	UD	UD	GND	UD	UD	UD	UD	GND
11	UD	UD	UD	UD	UD	GND	UD	UD	UD
12	GND	UD	UD	GND	UD	UD	UD	UD	GND
13	UD	UD	UD	UD	UD	GND	UD	UD	UD
14	GND	UD	UD	GND	UD	UD	UD	UD	GND
15	UD	UD	UD	UD	UD	GND	UD	UD	UD
16	GND	UD	UD	GND	UD	UD	UD	UD	GND

Payload Slot Profile with optical SLT3-PAY-2F2U1E-14.6.10— P1 & J1

Plug-in module P1			Row G	Row F	Row E Even	Row E Odd	Row D	Row C	Row B Even	Row B Odd	Row A
Bplane J1			Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Data Plane Port 1	X8 x4 / 2x2 / 4x1	GDiscrete1	GND	GND-J1	DP01-TD0-	DP01-TD0+	GND	GND-J1	DP01-RD0-	DP01-RD0+
2			GND	DP01-TD1-	DP01-TD1+	GND-J1	GND	DP01-RD1-	DP01-RD1+	GND-J1	GND
3			P1-VBAT	GND	GND-J1	DP01-TD2-	DP01-TD2+	GND	GND-J1	DP01-RD2-	DP01-RD2+
4			GND	DP01-TD3-	DP01-TD3+	GND-J1	GND	DP01-RD3-	DP01-RD3+	GND-J1	GND
5	Data Plane Port 2	X4 / 2x2 / 4x1	SYS_CON*	GND	GND-J1	DP02-TD0-	DP02-TD0+	GND	GND-J1	DP02-RD0-	DP02-RD0+
6			GND	DP02-TD1-	DP02-TD1+	GND-J1	GND	DP02-RD1-	DP02-RD1+	GND-J1	GND
7			Reserved	GND	GND-J1	DP02-TD2-	DP02-TD2+	GND	GND-J1	DP02-RD2-	DP02-RD2+
8			GND	DP02-TD3-	DP02-TD3+	GND-J1	GND	DP02-RD3-	DP02-RD3+	GND-J1	GND
9	User Defined		UD	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
10			GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
11			UD	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
12			GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
13			UD	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
14			GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
15	Control Plane		Maskable Reset*	GND	GND-J1	CPutp02-TD-	CPutp02-TD+	GND	GND-J1	CPutp02-RD-	CPutp02-RD+
16			GND	CPutp01-TD-	CPutp01-TD+	GND-J1	GND	CPutp01-RD-	CPutp01-RD+	GND-J1	GND



Payload Slot Profile with optical SLT3-PAY-2F2U1E-14.6.10— P2 & J2

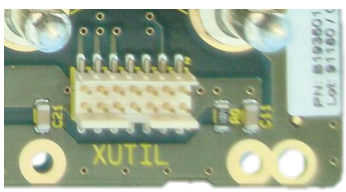
This connector is only a half-connector (wafers 1 to 0). It is all User Defined pins. See VITA 65.0 Section 6.3.3 for requirements and pin assignments
Concerning connectors that are all User Defined.
Connector Example Combined Plug-In Module & Backplane - Differential

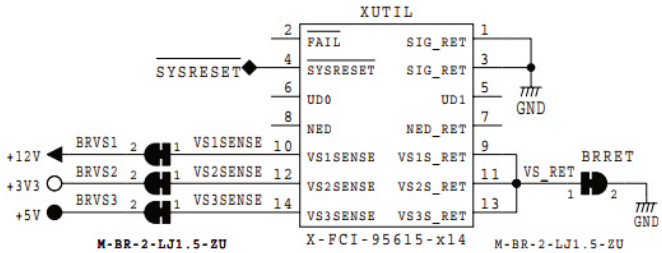
Backplane Jn	Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	UD	UD	UD	UD	UD	GND	UD	UD	UD
2	GND	UD	UD	GND	UD	UD	UD	UD	GND
3	UD	UD	UD	UD	UD	GND	UD	UD	UD
4	GND	UD	UD	GND	UD	UD	UD	UD	GND
5	UD	UD	UD	UD	UD	GND	UD	UD	UD
6	GND	UD	UD	GND	UD	UD	UD	UD	GND
7	UD	UD	UD	UD	UD	GND	UD	UD	UD
8	GND	UD	UD	GND	UD	UD	UD	UD	GND
9	UD	UD	UD	UD	UD	GND	UD	UD	UD
10	GND	UD	UD	GND	UD	UD	UD	UD	GND
11	UD	UD	UD	UD	UD	GND	UD	UD	UD
12	GND	UD	UD	GND	UD	UD	UD	UD	GND
13	UD	UD	UD	UD	UD	GND	UD	UD	UD
14	GND	UD	UD	GND	UD	UD	UD	UD	GND
15	UD	UD	UD	UD	UD	GND	UD	UD	UD
16	GND	UD	UD	GND	UD	UD	UD	UD	GND

5) Current Capability:

- +12V 42 A
- +3.3V 42 A
- +5V 45 A
- -12V AUX 3 A
- +12V AUX 3 A
- +3.3V AUX 3 A

6) UTILITY (Connector XUTIL)



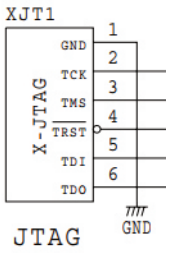




7) JTAG (Connector XJT1)



Consider: JTAG only at Slot 1, Payload slot



8) SYSCON

By setting the signal Syscon to GND the system slot is defined. In general the system slot is slot 1.

There are additional connector X_SC23 so as you can select any slot as system slot

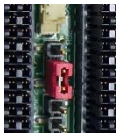
We offer 2 options for setting:

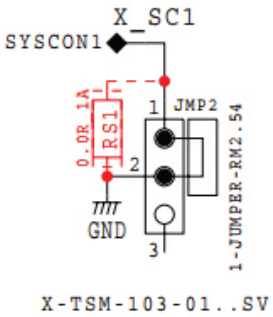
- Jumper (standard)

- 0 Ohm Resistor for rugged applications

X_SC12

1	SYSCON1
2	GND
3	SYSCON2





9) I2C Connector

There are 2 connectors for system-management I2CA and I2CB.

For customer specific board assembly Zero-Ohm resistors available.

Usable voltages for I2C are 3.3V-AUX

I2CA

1	I2CA_SCL
2	GND
3	I2CA_SDA
4	I2CA_PWR
5	NC

I2CB

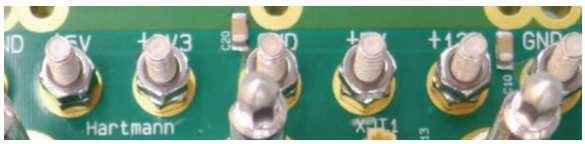
1	I2CB_SCL
2	GND
3	I2CB_SDA
4	I2CB_PWR
5	NC



10) Power Connections via M3 studs

The main operating voltages and GND are supplied with M3 studs.

The auxiliary operating voltages are supplied via 6 pole plug connector. Optimal daughter board supply and trouble-free operation are ensured by the arrangement of the feed modules on the backplane.

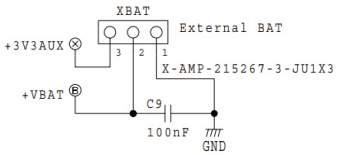


11) XBAT

Normally a battery voltage with approximately 3V is available at Pin VBAT of connector VPX-J1. The voltage is externally accessible with connector XBAT, Pin2 **or** internally using 3.3V_AUX by setting a Jumper between Pin2 and Pin3.

XBAT

1	GND
2	+VBAT
3	+3.3V_AUX

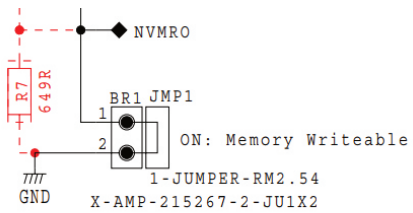


12) NVMRO

If Jumper BR1 is closed NVRMO is set to memory writeable.

BR1

1	NVMRO
2	GND



All data is for information purposes only and not guaranteed for legal purposes. Information has been carefully checked and is believed to be accurate; however, no responsibility is assumed for inaccuracies. Specifications are subject to change without notice.