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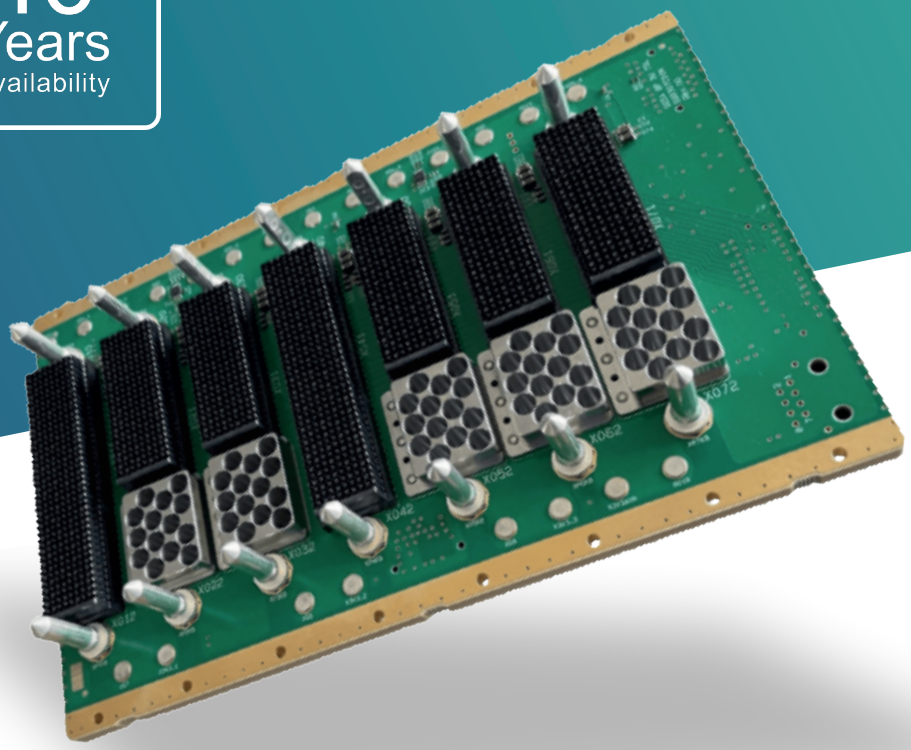
3U – 6U SOSA™ Aligned VPX Backplanes

Made in Germany

10 Years Availability



Size

3U form factor, SOSA™ aligned

Slots

7 slots (1 SBC, 1 Switch, 1 Clock, 4 Payload)

Input Voltage

DC feed via M3 screw terminals (VS1 12 V, VS2 3.3 V, VS3 5 V)

Permissible Current Load

VS1 = 120 A, VS2 = 90 A, VS3 = 90 A

Power Output Feeds

+12 V / +3.3 V / +5 V main, ±12 V AUX (7 A each), +3.3 V AUX (7 A)

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3U SOSA™ Aligned VPX Backplane 7 Slots

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VPX is a broadly defined technology utilizing the latest in a variety of switch fabric technologies in 3U and 6U format blades. Open VPX is the architecture framework that defines system-level VPX interoperability for multi-vendor, multi-module, integrated system environments.

The Open VPX framework defines clear interoperability points necessary for integration between Module to Module, Module to Backplane and Chassis. Open VPX recommends, but does not specify, development systems to assist evaluation, prototype and development of VPX systems. Open VPX will evolve and include new fabric, connector and system technology as newer standards are defined.

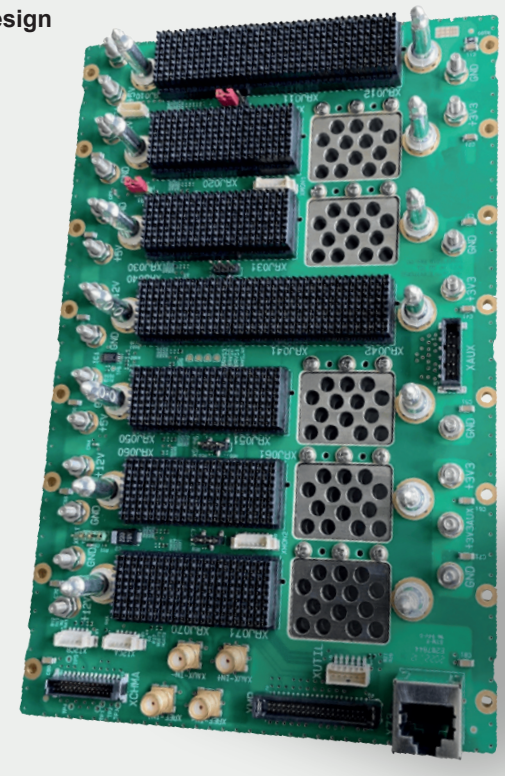
Hartmann Electronic's VPX Standard Backplanes are designed to allow any COTS or customer-specific configuration in either 3U or 6U form factor by providing a wide range of available VPX and OpenVPX profiles.

All Hartmann Backplanes support at least 1 Gbit Ethernet; most support 10 Gbit Ethernet, and the latest designs handle 100 Gbit Ethernet and PCIe Gen 4.

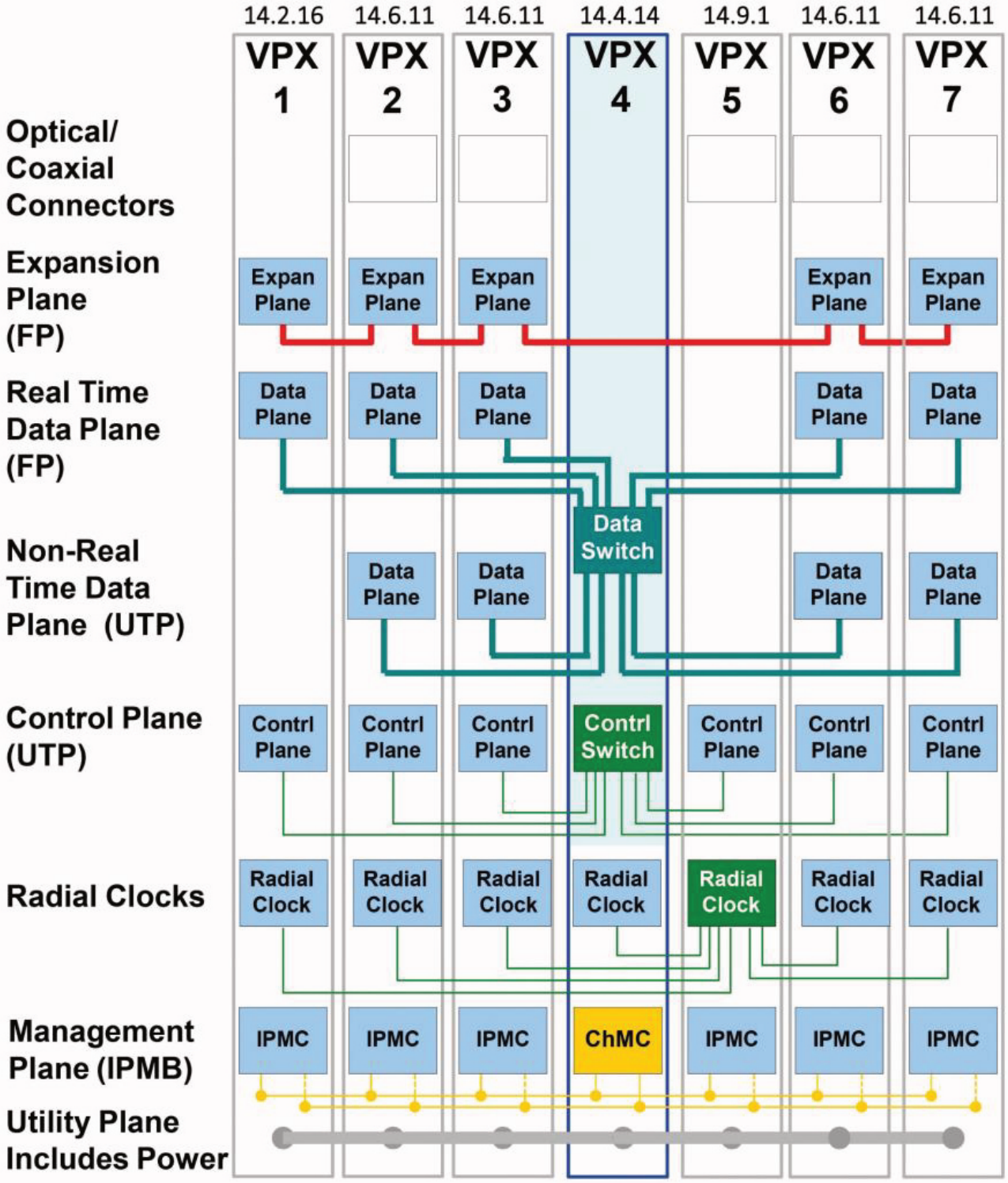
Using a modular concept based on open standards, it is common practice in the civil sector to integrate subsystem components from different manufacturers into a single modular system. The SOSA™ Technical Standard aims at such interoperability in embedded computing for military applications. A consortium of government, academic and private-sector enterprises – led by the U.S. Department of Defense – developed the SOSA™ Technical Standard as a COTS-based open standard providing reconfigurable, rapidly upgradable and cost-effective embedded computing capabilities. Based on OpenVPX, this architecture enables integration and interoperability of components using a modular approach for embedded system design.

Features:

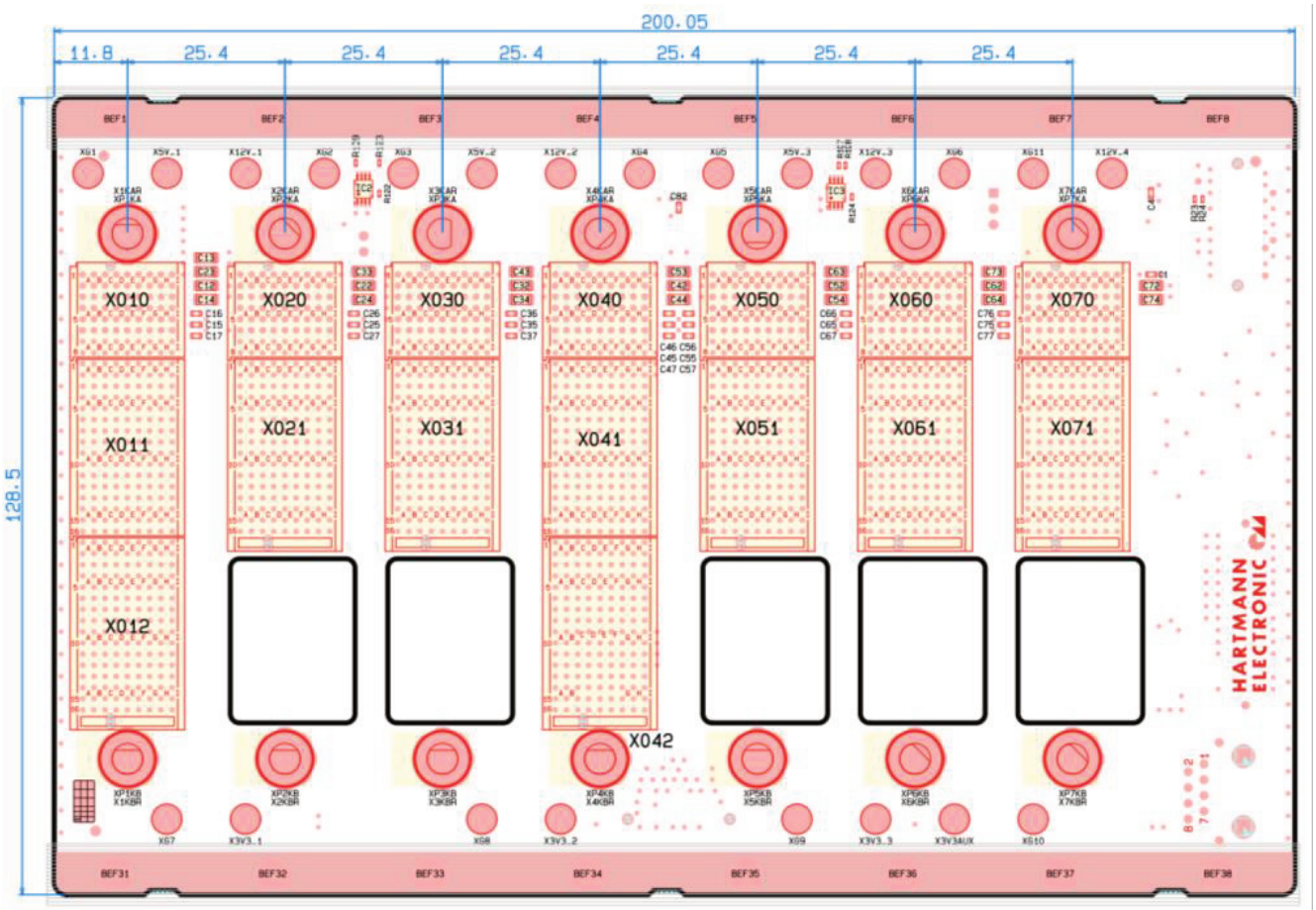
- High-speed 100 Gbit/s Ethernet (100GBase-KR4) design
- MULTIGIG RT 3 connectors by TE Connectivity
- SOSA™ / OpenVPX compliance (VITA 46 & 65)
- 7 slots: 1 SBC, 1 Switch, 1 Clock, 4 Payload Slots
- Optional VITA 67.3C coaxial modules
- M3 screw terminals for power entry
- JTAG and dual I²C management interfaces
- Flexible keying and geographical addressing
- Operating temperature −40 °C to +85 °C
- Custom assembly or modifications on request



Block Diagram



Drawings


200.05
11.8
25.4
25.4
25.4
25.4
25.4
25.4
128.5
X010
X020
X030
X040
X050
X060
X070
X011
X021
X031
X041
X051
X061
X071
X012
X042
HARTMANN ELECTRONIC


XCHMA
XBAT
XJT1
XRJ070
XRJ060
XRJ050
XRJ040
XRJ030
XRJ020
XRJ010
XRJ071
XRJ061
XRJ051
XRJ041
XRJ031
XRJ021
XRJ011
XRJ042
XRJ012
XMP
XUTIL
X73
XAUX
+12V
+5V
+3V3
GND

Pin Assignment

Pin AssignmentVPX J0 (Utility Connector)

	Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Vs1	Vs1	Vs1	Vs1	No Pad*	Vs2	Vs2	Vs2	Vs2
2	Vs1	Vs1	Vs1	Vs1	No Pad*	Vs2	Vs2	Vs2	Vs2
3	Vs3	Vs3	Vs3	Vs3	No Pad*	Vs3	Vs3	Vs3	Vs3
4	GND	SM2	SM3	GND	-12V_Aux	GND	SYSRESET*	NVMRO	GND
5	GND	GAP*	GA4*	GND	3.3V_Aux	GND	SM0	SM1	GND
6	GND	GA3*	GA2*	GND	+12V_Aux	GND	GA1*	GA0*	GND
7	TCK	GND	GND	TDO	TDI	GND	GND	TMS	TRST*
8	GND	REF_CLK-	REF_CLK+	GND	GND	AUX_CLK-	AUX_CLK+	GND	GND

VS1=12V , VS2=3.3V , VS3=5V

SBC Slot Profile SLT3-PAY-1F1F2U1TU1T1U1T-14.2.16 —P1 & J1

Plug-in module P1			Row G	Row F	Row E Even	Row E Odd	Row D	Row C	Row B Even	Row B Odd	Row A
Bplane J1			Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Data Plane	x4 / 2x2 / 4x1	GDiscrete1	GND	GND-J1	DP01-TD0-	DP01-TD0+	GND	GND-J1	DP01-RD0-	DP01-RD0+
2			GND	DP01-TD1-	DP01-TD1+	GND-J1	GND	DP01-RD1-	DP01-RD1+	GND-J1	GND
3			P1-VBAT	GND	GND-J1	DP01-TD2-	DP01-TD2+	GND	GND-J1	DP01-RD2-	DP01-RD2+
4			GND	DP01-TD3-	DP01-TD3+	GND-J1	GND	DP01-RD3-	DP01-RD3+	GND-J1	GND
5	Expansion Plane	x4 / 2x2 / 4x1	SYS_CON*	GND	GND-J1	EP00-TD-	EP00-TD+	GND	GND-J1	EP00-RD-	EP00-RD+
6			GND	EP01-TD-	EP01-TD+	GND-J1	GND	EP01-RD-	EP01-RD+	GND-J1	GND
7			USB01-VBUS	GND	GND-J1	EP02-TD-	EP02-TD+	GND	GND-J1	EP02-RD-	EP02-RD+
8			GND	EP03-TD-	EP03-TD+	GND-J1	GND	EP03-RD-	EP03-RD+	GND-J1	GND
9	X12d XMC mapping		MP01-TD	GND	GND-J1	XMCJ16-A5	XMCJ16-B5	GND	GND-J1	XMCJ16-D5	XMCJ16-E5
10			GND	XMCJ16-A7	XMCJ16-B7	GND-J1	GND	XMCJ16-D7	XMCJ16-E7	GND-J1	GND
11			MP01-RD	GND	GND-J1	XMCJ16-A9	XMCJ16-B9	GND	GND-J1	XMCJ16-D9	XMCJ16-E9
12			GND	XMCJ16-A15	XMCJ16-B15	GND-J1	GND	XMCJ16-D15	XMCJ16-E15	GND-J1	GND
13			GPIO1	GND	GND-J1	XMCJ16-A17	XMCJ16-B17	GND	GND-J1	XMCJ16-D17	XMCJ16-E17
14			GND	XMCJ16-A19	XMCJ16-B19	GND-J1	GND	XMCJ16-D19	XMCJ16-E19	GND-J1	GND
15	Control Plane		Maskable Reset*	GND	GND-J1	CPutp02-TD-	CPutp02-TD+	GND	GND-J1	CPutp02-RD-	CPutp02-RD+
16			GND	CPutp01-TD-	CPutp01-TD+	GND-J1	GND	CPutp01-RD-	CPutp01-RD+	GND-J1	GND

Pin Assignment

SBC Slot Profile SLT3-PAY-1F1F2U1TU1T1U1T-14.2.16 —P2 & J2

Plug-In Mod P2		Row G	Row F	Row E		Row D	Row C	Row B		Row A
				Even	Odd			Even	Odd	
Bplane J2		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	IO Block 1 – 8 wafers	SER01-TX-	GND	GND-J2	VID01-D1-	VID01-D1+	GND	GND-J2	VID01-D0-	VID01-D0+
2		GND	VID01-D3-	VID01-D3+	GND-J2	GND	VID01-D2-	VID01-D2+	GND-J2	GND
3		SER01-TX+	GND	GND-J2	VID01-PWR	VID01-HPD	GND	GND-J2	VID01-AUX-	VID01-AUX+
4		GND	USB02-D-	USB02-D+	GND-J2	GND	USB01-D-	USB01-D+	GND-J2	GND
5		SER01-RX-	GND	GND-J2	USB01-SST-	USB01-SST+	GND	GND-J2	USB01-SSR-	USB01-SSR+
6		GND	STRutp01-TD-	STRutp01-TD+	GND-J2	GND	STRutp01-RD-	STRutp01-RD+	GND-J2	GND
7		SER01-RX+	GND	GND-J2	CPtp01-DB-	CPtp01-DB+	GND	GND-J2	CPtp01-DA-	CPtp01-DA+
8		GND	CPtp01-DD-	CPtp01-DD+	GND-J2	GND	CPtp01-DC-	CPtp01-DC+	GND-J2	GND
9	X16s XMC map	USB02-VBUS	GND	GND-J2	XMCJ16-C12	XMCJ16-C13	GND	GND-J2	XMCJ16-F12	XMCJ16-F13
10		GND	XMCJ16-C14	XMCJ16-C15	GND-J2	GND	XMCJ16-F14	XMCJ16-F15	GND-J2	GND
11		GPIO2	GND	GND-J2	XMCJ16-C16	XMCJ16-C17	GND	GND-J2	XMCJ16-F16	XMCJ16-F17
12		GND	XMCJ16-C18	XMCJ16-C19	GND-J2	GND	XMCJ16-F18	XMCJ16-F19	GND-J2	GND
13	X8d XMC map	GPIO3	GND	GND-J2	XMCJ16-A1	XMCJ16-B1	GND	GND-J2	XMCJ16-D1	XMCJ16-E1
14		GND	XMCJ16-A3	XMCJ16-B3	GND-J2	GND	XMCJ16-D3	XMCJ16-E3	GND-J2	GND
15		GPIO4	GND	GND-J2	XMCJ16-A11	XMCJ16-B11	GND	GND-J2	XMCJ16-D11	XMCJ16-E11
16		GND	XMCJ16-A13	XMCJ16-B13	GND-J2	GND	XMCJ16-D13	XMCJ16-E13	GND-J2	GND

Switch Slot Profile SLT3-SWH-6F1U7U-14.4.14 —P1 & J1

Plug-In Module P1		Row G	Row F	Row E		Row D	Row C	Row B		Row A
				Even	Odd			Even	Odd	
Bplane J1		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Data Plane stacking Port	GDiscrete1	GND	GND-J1	DS01-TD0-	DS01-TD0+	GND	GND-J1	DS01-RD0-	DS01-RD0+
2		GND	DS01-TD1-	DS01-TD1+	GND-J1	GND	DS01-RD1-	DS01-RD1+	GND-J1	GND
3		P1-VBAT	GND	GND-J1	DS01-TD2-	DS01-TD2+	GND	GND-J1	DS01-RD2-	DS01-RD2+
4		GND	DS01-TD3-	DS01-TD3+	GND-J1	GND	DS01-RD3-	DS01-RD3+	GND-J1	GND
5	Data Plane Port 1	SYS_CON*	GND	GND-J1	DP01-TD0-	DP01-TD0+	GND	GND-J1	DP01-RD0-	DP01-RD0+
6		GND	DP01-TD1-	DP01-TD1+	GND-J1	GND	DP01-RD1-	DP01-RD1+	GND-J1	GND
7		Reserved	GND	GND-J1	DP01-TD2-	DP01-TD2+	GND	GND-J1	DP01-RD2-	DP01-RD2+
8		GND	DP01-TD3-	DP01-TD3+	GND-J1	GND	DP01-RD3-	DP01-RD3+	GND-J1	GND
9	Data Plane Port 2	MP01-TD	GND	GND-J1	DP02-TD0-	DP02-TD0+	GND	GND-J1	DP02-RD0-	DP02-RD0+
10		GND	DP02-TD1-	DP02-TD1+	GND-J1	GND	DP02-RD1-	DP02-RD1+	GND-J1	GND
11		MP01-RD	GND	GND-J1	DP02-TD2-	DP02-TD2+	GND	GND-J1	DP02-RD2-	DP02-RD2+
12		GND	DP02-TD3-	DP02-TD3+	GND-J1	GND	DP02-RD3-	DP02-RD3+	GND-J1	GND
13	Data Plane Port 3	Reserved	GND	GND-J1	DP03-TD0-	DP03-TD0+	GND	GND-J1	DP03-RD0-	DP03-RD0+
14		GND	DP03-TD1-	DP03-TD1+	GND-J1	GND	DP03-RD1-	DP03-RD1+	GND-J1	GND
15		Maskable Reset*	GND	GND-J1	DP03-TD2-	DP03-TD2+	GND	GND-J1	DP03-RD2-	DP03-RD2+
16		GND	DP03-TD3-	DP03-TD3+	GND-J1	GND	DP03-RD3-	DP03-RD3+	GND-J1	GND

Pin Assignment

Switch Slot Profile SLT3-SWH-6F1U7U-14.4.14 —P2 & J2

Plug-In Module P2		Row G	Row F	Row E Even	Row E Odd	Row D	Row C	Row B Even	Row B Odd	Row A
Bplane J2		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Data Plane Port 4	Reserved	GND	GND-J2	DP04-TD0-	DP04-TD0+	GND	GND-J2	DP04-RD0-	DP04-RD0+
2		GND	DP04-TD1-	DP04-TD1+	GND-J2	GND	DP04-RD1-	DP04-RD1+	GND-J2	GND
3		Reserved	GND	GND-J2	DP04-TD2-	DP04-TD2+	GND	GND-J2	DP04-RD2-	DP04-RD2+
4		GND	DP04-TD3-	DP04-TD3+	GND-J2	GND	DP04-RD3-	DP04-RD3+	GND-J2	GND
5	Data Plane Port 5	Reserved	GND	GND-J2	DP05-TD0-	DP05-TD0+	GND	GND-J2	DP05-RD0-	DP05-RD0+
6		GND	DP05-TD1-	DP05-TD1+	GND-J2	GND	DP05-RD1-	DP05-RD1+	GND-J2	GND
7		Reserved	GND	GND-J2	DP05-TD2-	DP05-TD2+	GND	GND-J2	DP05-RD2-	DP05-RD2+
8		GND	DP05-TD3-	DP05-TD3+	GND-J2	GND	DP05-RD3-	DP05-RD3+	GND-J2	GND
9	GND	GND	GND	GND-J2	GND	GND	GND	GND-J2	GND	GND
10	7 Control Plane one of which is stacking	GND	CSutp01-TD-	CSutp01-TD+	GND-J2	GND	CSutp01-RD-	CSutp01-RD+	GND-J2	GND
11		MP02-TD	GND	GND-J2	CPutp04-TD-	CPutp04-TD+	GND	GND-J2	CPutp04-RD-	CPutp04-RD+
12		GND	CPutp03-TD-	CPutp03-TD+	GND-J2	GND	CPutp03-RD-	CPutp03-RD+	GND-J2	GND
13		MP02-RD	GND	GND-J2	CPutp02-TD-	CPutp02-TD+	GND	GND-J2	CPutp02-RD-	CPutp02-RD+
14		GND	CPutp01-TD-	CPutp01-TD+	GND-J2	GND	CPutp01-RD-	CPutp01-RD+	GND-J2	GND
15		Reserved	GND	GND-J2	CPutp06-TD-	CPutp06-TD+	GND	GND-J2	CPutp06-RD-	CPutp06-RD+
16		GND	CPutp05-TD-	CPutp05-TD+	GND-J2	GND	CPutp05-RD-	CPutp05-RD+	GND-J2	GND

Clock Slot Profile SLT3x-TIM-4S16S1U2U1H-14.9.1 —P1 & J1

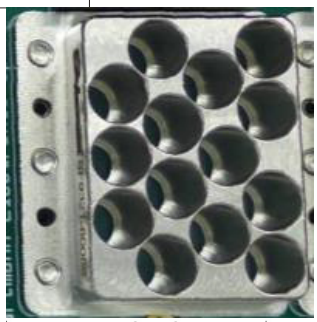
Plug-In Module P1		Row G	Row F	Row E Even	Row E Odd	Row D	Row C	Row B Even	Row B Odd	Row A
Bplane J1		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Ext clk/time inputs	GDiscrete1	GND	GND-J1	REF_RCLK-IN-	REF_RCLK-IN+	GND	GND-J1	AUX_RCLK-IN-	AUX_RCLK-IN+
2		GND	UD_timing-IN1-	UD_timing-IN1+	GND-J1	GND	UD_timing-IN2-	UD_timing-IN2+	GND-J1	GND
3	AUX_RCLK & REF_RCLK outputs 01 - 08	P1-VBAT	GND	GND-J1	AUX_RCLK01-	AUX_RCLK01+	GND	GND-J1	REF_RCLK01-	REF_RCLK01+
4		GND	AUX_RCLK02-	AUX_RCLK02+	GND-J1	GND	REF_RCLK02-	REF_RCLK02+	GND-J1	GND
5		SYS_CON*	GND	GND-J1	AUX_RCLK03-	AUX_RCLK03+	GND	GND-J1	REF_RCLK03-	REF_RCLK03+
6		GND	AUX_RCLK04-	AUX_RCLK04+	GND-J1	GND	REF_RCLK04-	REF_RCLK04+	GND-J1	GND
7		RSVD	GND	GND-J1	AUX_RCLK05-	AUX_RCLK05+	GND	GND-J1	REF_RCLK05-	REF_RCLK05+
8		GND	AUX_RCLK06-	AUX_RCLK06+	GND-J1	GND	REF_RCLK06-	REF_RCLK06+	GND-J1	GND
9		MP01-TD	GND	GND-J1	AUX_RCLK07-	AUX_RCLK07+	GND	GND-J1	REF_RCLK07-	REF_RCLK07+
10		GND	AUX_RCLK08-	AUX_RCLK08+	GND-J1	GND	REF_RCLK08-	REF_RCLK08+	GND-J1	GND
11	User Defined	MP01-RD	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
12		GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
13		RSVD	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
14	GND	GND	GND	GND	GND-J1	GND	GND	GND	GND-J1	GND
15	Control Plane	MaskableReset*	GND	GND-J1	CPutp02-TD-	CPutp02-TD+	GND	GND-J1	CPutp02-RD-	CPutp02-RD+
16		GND	CPutp01-TD-	CPutp01-TD+	GND-J1	GND	CPutp01-RD-	CPutp01-RD+	GND-J1	GND

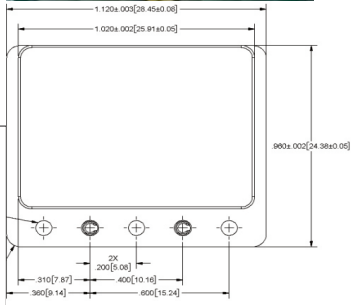
Pin Assignment

Switch Slot Profile SLT3-SWH-6F1U7U-14.4.14 —P2 &

The P2/J2 locaČon can be equipped with a VITA 67.3 type C Connector Module, any other Connector Module which fits in an Aperture PaĞern H locaČon or leǴ empty.

Coaxial Backplane Module e.g.part number SF9321-60086 by Amphenol.





Payload Slot Profile SLT3-PAY-1F1U1S1S1U1U2F1H-14.6.11 —P1 & J1

Plug-in module P1		Row G	Row F	Row E Even	Row E Odd	Row D	Row C	Row B Even	Row B Odd	Row A
Bplane J1		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Data Plane FP	GDiscrete1	GND	GND-J1	DP01-TD0-	DP01-TD0+	GND	GND-J1	DP01-RD0-	DP01-RD0+
2		GND	DP01-TD1-	DP01-TD1+	GND-J1	GND	DP01-RD1-	DP01-RD1+	GND-J1	GND
3		P1-VBAT	GND	GND-J1	DP01-TD2-	DP01-TD2+	GND	GND-J1	DP01-RD2-	DP01-RD2+
4		GND	DP01-TD3-	DP01-TD3+	GND-J1	GND	DP01-RD3-	DP01-RD3+	GND-J1	GND
5	Data Plane	SYS_CON*	GND	GND-J1	DPutp01-TD-	DPutp01-TD+	GND	GND-J1	DPutp01-RD-	DPutp01-RD+
6	GP, MP	GND	CLK1orGP-	CLK1orGP+	GND-J1	GND	MP01-TD	MP01-RD	GND-J1	GND
7	Ground	GND	GND	GND-J1	GND	GND	GND	GND-J1	GND	GND
8	Control Plane	GND	CPutp01-TD-	CPutp01-TD+	GND-J1	GND	CPutp01-RD-	CPutp01-RD+	GND-J1	GND
9	Expansion Plane Lanes 3:0	MP02-TD	GND	GND-J1	EP00-TD-	EP00-TD+	GND	GND-J1	EP00-RD-	EP00-RD+
10		GND	EP01-TD-	EP01-TD+	GND-J1	GND	EP01-RD-	EP01-RD+	GND-J1	GND
11		MP02-RD	GND	GND-J1	EP02-TD-	EP02-TD+	GND	GND-J1	EP02-RD-	EP02-RD+
12		GND	EP03-TD-	EP03-TD+	GND-J1	GND	EP03-RD-	EP03-RD+	GND-J1	GND
13	Expansion Plane Lanes 7:4	GPIO1	GND	GND-J1	EP04-TD-	EP04-TD+	GND	GND-J1	EP04-RD-	EP04-RD+
14		GND	EP05-TD-	EP05-TD+	GND-J1	GND	EP05-RD-	EP05-RD+	GND-J1	GND
15		Maskable Reset*	GND	GND-J1	EP06-TD-	EP06-TD+	GND	GND-J1	EP06-RD-	EP06-RD+
16		GND	EP07-TD-	EP07-TD+	GND-J1	GND	EP07-RD-	EP07-RD+	GND-J1	GND

Payload Slot Profile SLT3-PAY-1F1U1S1S1U1U2F1H-14.6.11 —P2 & J2

The P2/J2 locaČon can be equipped with a VITA 67.3 type C Connector Module, any other Connector Module which fits in an Aperture PaĞern H locaČon or leǴ empty.

Coaxial Backplane Module e.g.part number SF9321-60086 by Amphenol.

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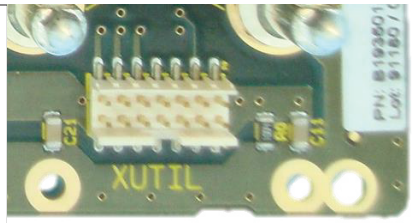
Coaxial Backplane Module e.g.part number SF9321-60086 by Amphenol.

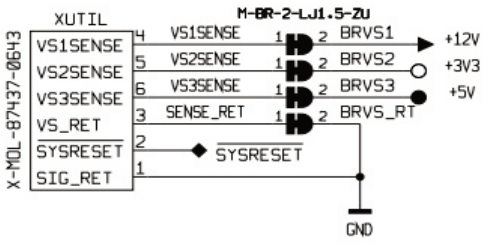
3U SOSA™ Aligned VPX Backplane 7 Slots

Current Capability:

+12V	120 A
+3.3V	90 A
+5V	90 A
-12V	AUX 7 A
+12V	AUX 7 A



UTILITY (Connector XUTIL)

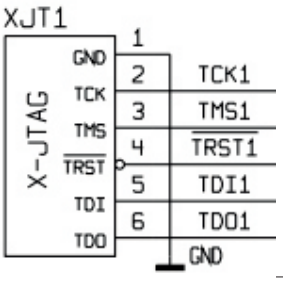


Connector Molex

87437-0643

JTAG (Connector XJT1)





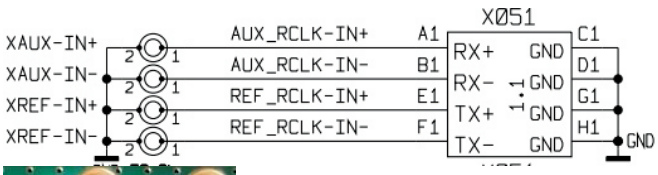
Connector JST

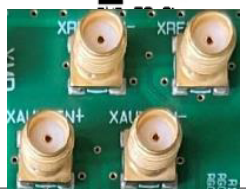
BM06B-SRSS-TB

Consider: JTAG only at Slot 1

Clock signals (Connectors XREF-in, XAUX-in)

As an external Čming input, the two differenČal reference clock signals REF_CLK and AUX_CLK can be supplied via four SMA connectors on the backplane.





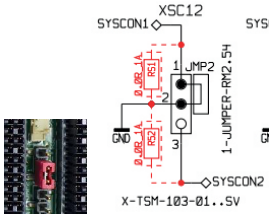
SYSCON

X_SC12
1 SYSCON1
2 GND
3 SYSCON2

By seŁ ng the signal Syscon to GND the system slot is defined. In generalthe system slot is slot 1.

There are addiČonal connectors X_SC34, X_SC56, X_SC7 so you can select any slot as system slot

We offer 2 opČons for seŁ ng: Jumper (standard) & 0 Ohm Resistor for rugged applicaČons



3U SOSA™ Aligned VPX Backplane 7 Slots

I2C Connector

There are 2 connectors for system-management I2CA and I2CB.

ForcustomerspecificboardassemblyZero-Ohmresistorsavailable.

UsablevoltagesforI2Care3.3V-AUX

I2CA

1	I2CA_SCL
2	GND
3	I2CA_SDA
4	I2CA_PWR
5	NC

I2CB

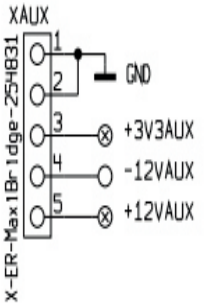
1	I2CB_SCL
2	GND
3	I2CB_SDA
4	I2CB_PWR
5	NC

Connector Molex 53398-0510

Power Studs M3 / AUX

The main operaČng voltages (+12V, 3.3V,+5V) and GND are supplied with M3 screw terminals.

The auxiliary operaČng voltages are supplied via M3 Screw terminal and via single row verČcal terminals. OpČmal daughter board supply and trouble-free operaČon are ensured by the arrangement of the feed modules on the backplane.



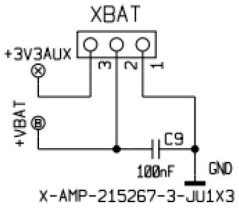


XBAT

Normally a baĞery voltage with approximately 3V is available at Pin VBAT of connector VPX-J1. The voltage is externally accessible with connector XBAT, Pin2 **or**internally using 3.3V_AUX by seł ng a Jumper between Pin2 and Pin3.

VBAT X5

1	GND
2	+VBAT
3	+3.3V_AUX



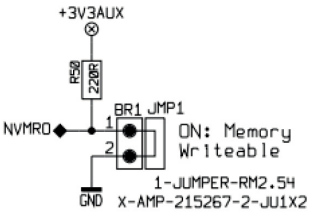
Connector AMP 215267-3

NVMRO

If Jumper BR1 is closed NVRMO is set to memory writeable.

BR1

1	NVMRO
2	GND



Technical Information

Article	Ordering Code	Description
3U – 6U SOSA™ Aligned VPX Backplanes	B143070011	1 SBC, 1 Switch, 1 Clock, 4 Payload slots Screw Terminal

Technical Information

Form Factor	3U
Slots	7
Slot Pitch	5HP
Topology	Centralized
Impedance Controlled	YES
Design	100GBase-KR4
Base Specification	in alignment with the SOSA™ Technical Standard
PCB Thickness	5.4 mm
Connectors	MultiGig RT3
Power Feed	Screw Terminal
Board Size	3U/6U
Chassis Height	3U

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